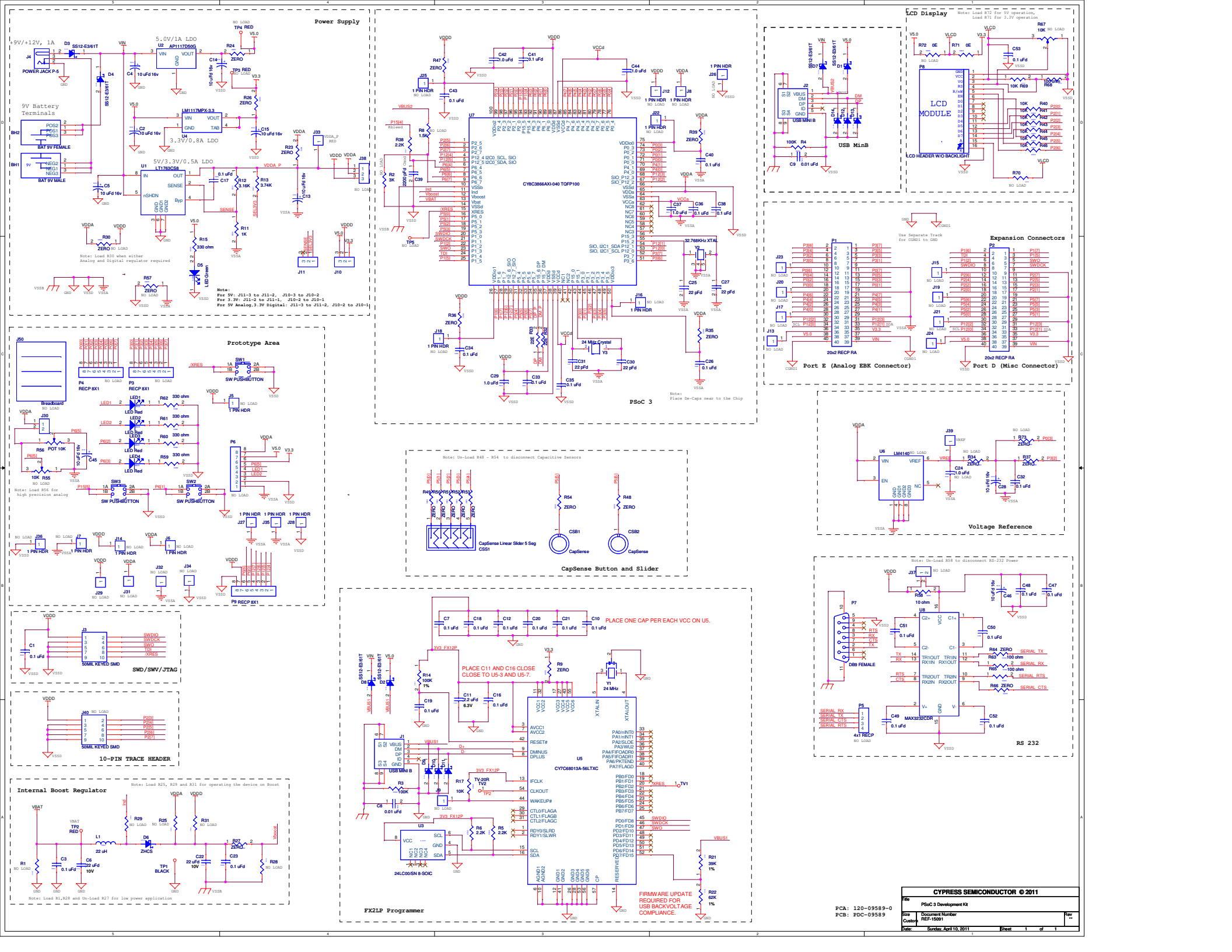
Power Supply
+9V/+12V, 1A
5.0V/1A LDO
AP1117D50G
3.3V/0.8A LDO
LM1117MPX-3.3
5V/3.3V/0.5A LDO
LT1763CS8
9V Battery Terminals
POWER JACK P-5
BAT 9V FEMALE
BAT 9V MALE
LED Green
Note: For 5V, J11-3 to J11-2, J10-3 to J10-2
For 3.3V, J11-2 to J11-1, J10-2 to J10-1
For 5V Analog,3.3V Digital: J11-3 to J11-2, J10-2 to J10-1
Prototype Area
Breadboard
RECP 8X1
SW PUSHBUTTON
POT 10K
Note: Run R56 for high precision analog
SWD/SWV/JTAG
50MIL KEYED SMD
10-PIN TRACE HEADER
Internal Boost Regulator
Note: Load R25, R29 and R31 for operating the device on Boost
Note: Load R1,R28 and Un-Load R27 for low power application
PSoC 3
CY8C3866AXI-040 TQFP100
Note: Place De-Caps near to the Chip
CapSense Button and Slider
Note: Un-Load R48 ~ R54 to disconnect Capacitive Sensors
CapSense Linear Slider 5 Seg
CapSense
FX2LP Programmer
CY7C68013A-56LTXC
24LC00/SN 8-SOIC
PLACE ONE CAP PER EACH VCC ON U5.
PLACE C11 AND C16 CLOSE CLOSE TO U5-3 AND U5-7.
FIRMWARE UPDATE REQUIRED FOR USB BACKVOLTAGE COMPLIANCE.
USB MiniB
USB MINI B
LCD Display
LCD MODULE
LCD HEADER W/O BACKLIGHT
Use Separate Track for CGND1 to GND
Expansion Connectors
Port E (Analog EBK Connector)
Port D (Misc Connector)
20x2 RECP RA
Voltage Reference
LM4140
RS 232
DB9 FEMALE
MAX3232CDR
4xT RECP
PCA: 120-09589-0
PCB: PDC-09589
CYPRESS SEMICONDUCTOR © 2011
PSoC 3 Development Kit
Document Number REF-15091
Sunday, April 10, 2011